

**What is claimed is:**

**[Claim 1]** 1. The low temperature polysilicon thin film transistor, comprising:

a substrate;  
a polysilicon layer, disposed over the substrate, the polysilicon layer comprising a lightly doped drain, a channel region inside the lightly doped drain region and a source/drain region outside the lightly doped drain region;  
a gate insulation layer, disposed over the substrate covering the polysilicon layer;  
a gate buffer layer, arranged over the gate insulation layer covering the channel region and the lightly doped drain;  
a gate, disposed over the gate buffer layer covering the channel region;  
a dielectric layer, arranged over the gate insulation layer covering the gate;  
a drain metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the drain region; and  
a source metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the source region.

**[Claim 2]** 2. The low temperature polysilicon thin film transistor of claim 1, wherein a material constituting the gate comprises a metal.

**[Claim 3]** 3. The low temperature polysilicon thin film transistor of claim 2, wherein a material constituting the gate buffer layer comprises a metallic compound.

**[Claim 4]** 4. The low temperature polysilicon thin film transistor of claim 3, wherein the metallic compound is selected from a group consisting of a metal oxide, a metal nitride and a metal carbide.

**[Claim 5]** 5. The low temperature polysilicon thin film transistor of claim 3, wherein the portion of the gate buffer layer nearer to the gate insulation layer has lower amount of metal.

[Claim 6] 6. The low temperature polysilicon thin fin transistor of claim 1, wherein a material constituting the gate buffer layer comprises a dopant containing material.

[Claim 7] 7. The low temperature polysilicon thin fin transistor of claim 6, wherein the portion of the gate buffer layer nearer to the gate insulation layer has more amount of dopant.

[Claim 8] 8. The low temperature polysilicon thin fin transistor of claim 1, wherein a portion of the lightly doped drain nearer to the source/drain region has a higher dopant concentration.

[Claim 9] 9. The low temperature polysilicon thin film transistor of claim 1, wherein a structure of the gate buffer layer is ladder-shape.

[Claim 10] 10. The low temperature polysilicon thin film transistor of claim 1, wherein a structure of the gate buffer layer is taper-shape.

[Claim 11] 11. The low temperature polysilicon thin film transistor of claim 1, further comprising a buffer layer arranged between the substrate and the polysilicon layer.

[Claim 12] 12. The method of fabricating a lightly doped drain region, comprising:

forming a polysilicon layer over a substrate;

forming a gate insulation layer over the polysilicon layer;

sequentially forming a gate buffer layer over the gate insulation layer and a gate over the gate buffer layer, wherein an edge portion of the gate buffer layer is exposed; and

performing a doping process to form a lightly doped drain region in the polysilicon layer underneath the exposed portion of the gate buffer layer.

[Claim 13] 13. The method of fabricating a lightly doped drain region of claim 12, wherein the steps of forming the gate buffer layer and the gate comprises:

forming a gate buffer material layer over the gate insulation layer and forming a gate material layer over the gate buffer layer; and

patterning the gate material layer and the gate buffer material layer to form the gate and the gate buffer layer using a photolithography process and an etching process, wherein an etching rate of the gate material is larger than that of the gate buffer material.

[Claim 14] 14. The method of fabricating a lightly doped drain region of claim 13, wherein the gate material is formed by a sputtering process and the gate buffer material layer is formed by a sputtering process containing a reactive gas.

[Claim 15] 15. The method of fabricating a lightly doped drain region of claim 14, wherein the reactive gas is selected from a group consisting of an oxygen containing gas, a nitrogen containing gas and a carbon containing gas.

[Claim 16] 16. The method of fabricating a lightly doped drain region of claim 14, wherein the reactive gas comprises a dopant containing gas.

[Claim 17] 17. The method of fabricating a lightly doped drain region of claim 14, wherein an amount of the reactive gas is decreased with time during the sputtering process.

[Claim 18] 18. The method of fabricating a lightly doped drain region of claim 12, further comprises a step of forming a buffer layer over the substrate before the step of forming the polysilicon layer over the substrate.